REMARKS

Claims 1, 3, 4, 6 and 20-29 are pending in the application. In the Office Action of April 24, 2002, the Examiner made the following disposition:

A.) Rejected claims 1, 3, 4, 6, and 20-26 under 35 U.S.C. §112, first paragraph.

B.) Rejected claims 3, 22, and 27-29 under 35 U.S.C. §112, first paragraph.

C.) Rejected claims 22 and 27-29 under 35 U.S.C. §112, second paragraph.

D.) Rejected claims 1, 3, 4, and 20-25 under 35 U.S.C. §102(b) as being anticipated by *Kumamaru et al.*

E.) Rejected claims 1, 3, 4, 21-23, and 25 under 35 U.S.C. §102(b) as being anticipated by *Watanabe et al.*

F.) Rejected claims 6 and 26 under 35 U.S.C. §103(a) as being unpatentable over *Watanabe et al.*

G.) Rejected claim 26 under 35 U.S.C. §103(a) as being unpatentable over *Kumamaru et al.*

H.) Rejected claims 6 and 27-29 under 35 U.S.C. §103(a) as being unpatentable over *Kumamaru et al.* in view of *Watanabe et al.*

Applicants respectfully traverse the rejections and addresses the Examiner's disposition as follows:

A.) Rejection of claims 1, 3, 4, 6, and 20-26 under 35 U.S.C. §112, first paragraph:

Claim 1 has been amended, as per the Examiner's request to overcome the rejection. Specifically, claim 1 has been amended to remove the text stating that the second embedded diffusion layer is --within a lower part of the epitaxial layer--. Attached hereto is a marked-up version of the changes made to the claims by the current amendment. The attached page is captioned **"VERSION WITH MARKING TO SHOW CHANGES MADE**.

Claims 3, 4, 6, and 20-26 depend directly or indirectly from claim 1 and are therefore allowable for at least the same reasons that claim 1 is allowable.

Applicants respectfully submit that the rejection has been overcome and request that it be withdrawn.

B.) Rejection of claims 3, 22, and 27-29 under 35 U.S.C. §112, first paragraph:

Claim 3 has been amended, as per the Examiner's request, to overcome the rejection. Specifically, claim 3 has been amended to clarify that the bottom of the second embedded diffusion layer is formed at a distance that is greater than a bottom of the first embedded diffusion layer. Support for this claim language can be found, for example, in Fig. 5.

Claim 22 has been amended, as per the Examiner's request to overcome the rejection. Specifically, claim 22 has been amended to clarify that a peak position of an impurity concentration of the second embedded diffusion layer resides at a distance from the surface of the emitter of the second vertical type bipolar transistor that is approximately equal to a location of the bottom of the first embedded diffusion layer from the surface of the emitter of the first vertical type bipolar transmitter. As can be seen in Figs. 5, 8O, and 8S, the surface of the emitters of the first and second vertical type bipolar transistors are formed at a same time at a same level. As illustratively depicted in Figs. 6 and 7, the peak position of the impurity concentration of the second embedded diffusion layer (Fig. 7, item 151) is approximately equal to the location of the bottom of the first embedded diffusion layer (Fig. 6, item 131).

Claim 27-29 have been cancelled.

Applicants respectfully submit that the rejection has been overcome and request that it be withdrawn.

C.) Rejection of claims 22 and 27-29 under 35 U.S.C. §112, second paragraph:

Claim 22 has been amended, as per the Examiner's request to overcome the rejection. Specifically, claim 22 has been amended to clarify that a peak position of an impurity concentration of the second embedded diffusion layer resides at a distance from the surface of the emitter of the second vertical type bipolar transistor that is approximately equal to a location of the bottom of the first embedded diffusion layer from the surface of the emitter of the first vertical type bipolar transmitter. As can be seen in Figs. 5, 8O, and 8S, the surface of the emitters of the first and second vertical type bipolar transistors are formed at a same time at a same level. As illustratively depicted in Figs. 6 and 7, the peak position of the impurity concentration of the second embedded diffusion layer (Fig. 7, item 151) is approximately equal to the location of the bottom of the first embedded diffusion layer (Fig. 6, item 131).

Claims 27-29 have been cancelled.

Applicants respectfully submit that the rejection has been overcome and request that it be withdrawn.

D.) Rejection of claims 1, 3, 4, and 20-25 under 35 U.S.C. §102(b) as being anticipated by *Kumamaru et al.*:

Applicants respectfully disagree with the rejection.

Applicants' independent claim 1 claims a semiconductor device having a substrate and an epitaxial layer formed on the substrate. A first embedded diffusion layer is formed in a first upper part of the substrate and in the epitaxial layer. A second embedded diffusion layer is formed in a second upper part of the substrate. The second embedded diffusion layer includes an impurity concentration that is less than the impurity concentration of the first embedded diffusion layer and is equal to or higher than that of the epitaxial layer.

The peak position of the impurity concentration of the first embedded diffusion layer resides at a first distance from a surface of an emitter of the first vertical type bipolar transistor, and a peak position of the impurity concentration of the second embedded diffusion layer resides at a second distance from a surface of an emitter of the second vertical type bipolar transistor. As illustratively depicted in Applicants' Fig. 5, the first distance is smaller than the second distance.

This is clearly unlike *Kumamaru et al.* To begin with, referring to *Kumamaru et al.* Fig. 10, *Kumamaru et al.*'s first embedded diffusion layer 15 is sandwiched between two epitaxial layers 5, 11. This is unlike Applicants' first embedded diffusion layer, which is formed in an upper part of a substrate and in an epitaxial layer. Nowhere does *Kumamaru et al.* disclose or even suggest that its first embedded diffusion layer is formed in its substrate 1.

Further, *Kumamaru et al.* fails to disclose a second embedded diffusion layer having an impurity concentration that is equal to or higher than that of an epitaxial layer. *Kumamaru et al.* discloses that its first and second epitaxial layers 5, 11 have impurity concentrations of 1×10^{14} to 5×10^{14}. (Col. 4, lines 14-17; col. 4, lines 21-25). *Kumamaru et al.'s* second embedded diffusion layer 13 is formed by the diffusion of phosphorous from its n^--type impurity region 10 into its p-type epitaxial layer 5. (Col. 3, lines 23-30). Since an impurity concentration of the n^--type impurity region 10 is 7×10^{11} to 1.2×10^{12} (Col. 4, lines 18-20), an impurity concentration of its second embedded diffusion layer 13 is less than 7×10^{11} to 1.2×10^{12} due to conversion between the impurity of the p-type and that of the n-type. Accordingly, *Kumamaru et al.'s* second embedded diffusion layer 13 has an impurity concentration of less than 7×10^{11} to 1.2×10^{12}, which is less than the impurity concentration *Kumamaru et al.'s* epitaxial layers at 1×10^{14} to 5×10^{14}. Therefore, unlike Applicants' claim 1, *Kimamaru et al.* fails to disclose an impurity

concentration of its second embedded diffusion layer that is equal to or higher than that of its epitaxial layer. So, for this reason also, *Kimamaru et al.* could not disclose or even suggest Applicants' claim 1.

Therefore, for at least the reasons stated above, *Kimamaru et al.* fails to disclose or even suggest Applicants' claim 1.

Claims 3, 4, and 20-25 depend directly or indirectly from claim 1 and are therefore allowable for at least the same reasons that claim 1 is allowable.

Applicants respectfully submit that the rejection has been overcome and request that it be withdrawn.

E.) Rejection of claims 1, 3, 4, 21-23, and 25 under 35 U.S.C. §102(b) as being anticipated by *Watanabe et al.*:

Applicants respectfully disagree with the rejection.

Applicants' independent claim 1 is described above. Further, Applicants' independent claim 1 claims a semiconductor device having a first vertical type bipolar transistor and a second vertical type bipolar transistor having a breakdown voltage that is higher than a breakdown voltage of the first vertical type bipolar transistor.

This is clearly unlike *Watanabe et al.* Unlike Applicants' claim 1, which claims first and second vertical type bipolar transistors, *Watanabe et al.* discloses a NPN bipolar transistor and an IIL (Integrated Injection Logic) device. Accordingly, unlike Applicants' claim 1, nowhere could *Watanabe et al.* disclose or even suggest a breakdown voltage of a second vertical type bipolar transistor that is higher than a breakdown voltage of a first vertical type bipolar transistor.

Referring to *Watanbabe et al.* Fig. 8, *Watanabe et al.'s* second embedded diffusion layer 22'' formed on its n-type layer 41' is close to its base region 52. Accordingly, even if the lower portion of the second embedded diffusion layer 22'' formed below the n-type layer 41' exists in *Watanabe et al.'s* IIL device, the breakdown voltage of the IIL device is determined by the upper portion of the second embedded diffusion layer 22''. Since the upper portion of the second embedded diffusion layer 22'' is formed on the n-type layer 41' so close to the base region 52, the breakdown voltage of *Watanabe et al.'s* IIL device is lower than that of *Watanabe et al.'s* NPN bipolar transistor. So, unlike Applicants' claim 1, *Watanabe et al.* fails to disclose or even suggest a breakdown voltage of a second vertical type bipolar transistor that is higher than a breakdown voltage of a first vertical type bipolar transistor.

Therefore, *Watanabe et al.* fails to disclose or even suggest Applicants' claim 1.

Claims 3, 4, 21-23, and 25 depend directly or indirectly from claim 1 and are therefore allowable for at least the same reasons that claim 1 is allowable.

Applicants respectfully submit that the rejection has been overcome and request that it be withdrawn.

F.) Rejection of claims 6 and 26 under 35 U.S.C. §103(a) as being unpatentable over *Watanabe et al.*:

Applicants respectfully disagree with the rejection.

Applicants' independent claim 1 is allowable over *Watanabe et al.* as described above.

Claims 6 and 26 depend directly or indirectly from claim 1 and are therefore allowable for at least the same reasons that claim 1 is allowable.

Applicants respectfully submit that the rejection has been overcome and request that it be withdrawn.

G.) Rejection of claim 26 under 35 U.S.C. §103(a) as being unpatentable over *Kumamaru et al.*:

Applicants respectfully disagree with the rejection.

Applicants' claim 1 is allowable over *Kumamaru et al.* as described above.

Claim 26 depends directly or indirectly from claim 1 and is therefore allowable for at least the same reasons that claim 1 is allowable.

Applicants respectfully submit that the rejection has been overcome and request that it be withdrawn.

H.) Rejection of claims 6 and 27-29 under 35 U.S.C. §103(a) as being unpatentable over *Kumamaru et al.* in view of *Watanabe et al.*:

Applicants respectfully disagree with the rejection.

Applicants' independent claim 1 is allowable over *Kumamaru et al.* and *Watanabe et al.* as described above. Further, claim 1 is allowable over *Kumamaru et al.* and *Watanabe et al.*, in combination, for at least the reasons described above.

Claim 6 depends directly or indirectly from claim 1 and is therefore allowable for at least the same reasons that claim 1 is allowable.

Claims 27-29 have been cancelled.

Applicants respectfully submit that the rejection has been overcome and request that it be withdrawn.

Claims 30-31 are newly added.

CONCLUSION

In view of the foregoing, it is submitted that claims 1, 3, 4, 6, 20-26, and 30-31 are patentable. It is therefore submitted that the application is in condition for allowance. Notice to that effect is respectfully requested.

Respectfully submitted,

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3. (Amended) A semiconductor device according to claim 1,

wherein a bottom of the first embedded diffusion layer is formed at a third distance from the [datum surface of the substrate] surface of the emitter of the first vertical type bipolar transistor, and

wherein a [midpoint] bottom of the second embedded diffusion layer is formed at a fourth distance from the [datum surface of the substrate] surface of the emitter of the second vertical type bipolar transistor such that the fourth distance is greater than the third distance.

6. (Amended) A semiconductor device according to claim 1, wherein the substrate is a single substrate, [wherein the datum surface is a bottom surface of the substrate,] and wherein the impurity concentration of the second embedded diffusion layer is $1x10^{13}$ to $1x10^{15}$.

22. (Amended) A semiconductor device according to claim 1, wherein a peak position of an impurity concentration of the second embedded diffusion layer resides at a distance from the [datum surface of the substrate] surface of the emitter of the second vertical type bipolar transistor that is approximately equal to a location of the bottom of the first embedded diffusion layer from the [datum surface of the substrate] surface of the emitter of the first vertical type bipolar transmitter.

Please cancel claims 27-29.

Please add the following new claims 30 and 31:

30. The semiconductor device of claim 1, wherein the first vertical type bipolar transistor is capable of operating at a higher speed than the second vertical type bipolar transistor.

31. The semiconductor device of claim 1, wherein the second vertical type bipolar transistor is capable of operating at a higher voltage than the first vertical type bipolar transistor.

VERSION WITH MARKINGS TO SHOW CHANGES MADE

In the Claims:

Please amend claims 1, 3, 6 and 22 as follows:

1. (Amended) A semiconductor device having a first vertical type bipolar transistor and a second vertical type bipolar transistor having a breakdown voltage that is higher than a breakdown voltage of the first vertical type bipolar transistor, said transistors each having an emitter, a base, and a collector, the semiconductor device comprising:

a substrate [defining a datum surface, wherein the substrate is] of a first conductive type [substrate];

an epitaxial layer formed on the substrate [above the datum surface];

a first embedded diffusion layer formed as a part of [a] the first vertical type bipolar transistor in a first upper part of the substrate and in the epitaxial layer;

a second embedded diffusion layer formed as a part of [a] the second vertical type bipolar transistor directly on the substrate, in a second upper part of the substrate[, and within a lower part of the epitaxial layer],

wherein the first embedded diffusion layer is not disposed within the second embedded diffusion layer,

wherein the second embedded diffusion layer is of a second conductive type [second embedded diffusion layer] that is a different conductive type from the first conductive type substrate and includes an impurity concentration that is less than [the] an impurity concentration of the first embedded diffusion layer and is equal to or higher than that of the epitaxial layer, and

wherein a peak position of [an] the impurity concentration of the first embedded diffusion layer resides at a first distance from [the datum surface of the substrate] a surface of the emitter of the first vertical type bipolar transistor and a peak position of [an] the impurity concentration of the second embedded diffusion layer resides at a second distance from [the datum surface of the substrate] a surface of the emitter of the second vertical type bipolar transistor such that the first distance is [greater] smaller than the second distance.

CERTIFICATE OF MAILING

I hereby certify that this correspondence is being deposited as First Class Mail in an envelope addressed to Asst. Commissioner for Patents, Washington, D.C. 20231 on September 23, 2002.

(Reg. No. 45,034)
Christopher P. Rauch